STATUS OF THE CLAIMS

This listing of claims replaces all prior listing of claims in this application.

1-38 (Canceled).

39. (Currently Amended) A processor system comprising:

a central processing unit; and

a memory device connected to said central processing unit, said memory device comprised of a plurality of low profile ball grid array semiconductor packages, said low profile ball grid array semiconductor packages comprised of a base substrate having a top surface and a bottom surface, with an aperture therein which extends from said top surface to said bottom surface,

a series of conductive traces located on one of said top surface and said bottom surface of said base substrate,

a plurality of conductive balls connected to said series of conductive traces,

a ~~single thin layer of~~ thin sheet material secured to said base substrate and covering said aperture such that a cavity is formed, said ~~single thin layer of~~ thin sheet material having a thickness of from approximately 0.025 to ~~less than approximately~~ 0.1 mm, and a semiconductor element mounted in said cavity.

40. (Previously Presented) The processor system according to claim 39, said single thin layer of material further comprising:

a polyimide based material.

41. (Previously Presented) The processor system according to claim 39, said single thin layer of material further comprising:

a metal foil based material.

42. (Currently Amended) A processor system comprising:

a central processing unit; and

a memory device connected to said central processing unit, said memory device comprised of a plurality of low profile ball grid array semiconductor packages, said low profile ball grid array semiconductor packages comprised of a base substrate having a top surface and a bottom surface, said base substrate having an aperture extending from said top surface to said bottom surface,

a series of conductive traces located on one of said top surface and said bottom surface of said base substrate,

a plurality of conductive balls connected to said series of conductive traces,

a ~~single thin layer of~~ thin sheet material secured to said top surface of said base substrate and covering said aperture to form a downward facing cavity, said ~~single thin layer of~~ thin sheet material having a thickness of from approximately 0.025 to ~~less than approximately~~ 0.1 mm, and a semiconductor element mounted in said downward facing cavity.

43. (Previously Presented) The processor system according to claim 42, said single thin layer of material further comprising:

a polyimide based material.

44. (Previously Presented) The processor system according to claim 39, said single thin layer of material further comprising:

a metal foil based material.

45. (currently amended) A processor system comprising:

a central processing unit; and

a memory device connected to said central processing unit, said memory device comprised of a plurality of low profile ball grid array semiconductor packages, said low profile ball grid array semiconductor packages comprised of a base substrate having a top surface and a bottom surface, with an aperture therein which extends from said top surface to said bottom surface,

a series of conductive traces located on one of said top surface and said bottom surface of said base substrate,

a plurality of conductive balls connected to said series of conductive traces,

a thin sheet material secured to said base substrate and covering said aperture such that a cavity is formed, said thin sheet material having a thickness of from approximately 0.025 to ~~less than approximately~~ 0.1 mm, and a semiconductor element mounted in said cavity.